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Discontinuous SVPWM Techniques for Balanced Two-Phase Three-Leg Voltage Source Inverter

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Abstract

This paper describes the balanced phase voltage Discontinuous Space Vector PWM (DSVPWM) techniques for three-leg voltage source inverter (VSI) supplying balanced two-phase loads. Proposed DSVPWM strategy focuses on an analysis of switching losses by dealing with various types of zero space vector time in each switching sequence at high modulation index. The minimum of reduction in the switching losses will be occurred at 30 degrees lagging load power factor when compared with a continuous SVPWM technique. These proposed techniques are implemented on TMS320F28335 eZdsp for generating PWM gating signals of the switching devices in the main power circuit. The simulation and experimental results are given under conditions of switching losses and output current ripple to verify the correctness of the proposed principle.

Keywords: Discontinuous SVPWM, Switching losses, Two-phase voltage source inverter, Two-phase loads

1. Introduction

Space vector pulse width modulation (SVPWM) is very popular for VSIs due to better characteristics such as wider linear modulation range, less total harmonic distortion (THD) and easier implementation. In order to improve the performance of a three-phase three-leg VSI in terms of reductions in switching losses and current ripple, previous works proposed discontinuous modulation which provided PWM patterns allowing one switching device for each phase leg without switching in a certain interval when compared to continuous modulation. Means of a reduction in power losses with discontinuous space vector PWM (DSVPWM) caused by semiconductors can be found in [1]. The requirement of such interval or clapping time is dependent of power factor of the load connected to the inverter output. Several papers proposed various types of DSVPWM such as 120^0 clamping classified as DPWMMIN and DPWMMAX,

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60^0 clamping classified as DPWM1, DPWM2 and DPWM0[3]-[4]. Similarly, Proposed DSVPWM techniques in this paper for balanced two-phase VSI can be implemented in the same manner as unbalanced two-phase VSI concept [2]. The objectives of this technique are to increase efficiency and performance not only the two-phase VSI but also the two-phase induction motor drive. In addition, these techniques offer switching losses and output current ripple at higher modulation index when compared to the CSVPWM technique. This paper focuses on the principle in details and analyzes DSVPWM using three-leg VSI for two-phase balanced RL loads. The proposed main power circuit is shown in Fig. 1. Each phase has 30 lagging power factor. The simulation and experimental results are given under testing conditions of switching losses and output current ripple to verify the correctness of the proposed principle.

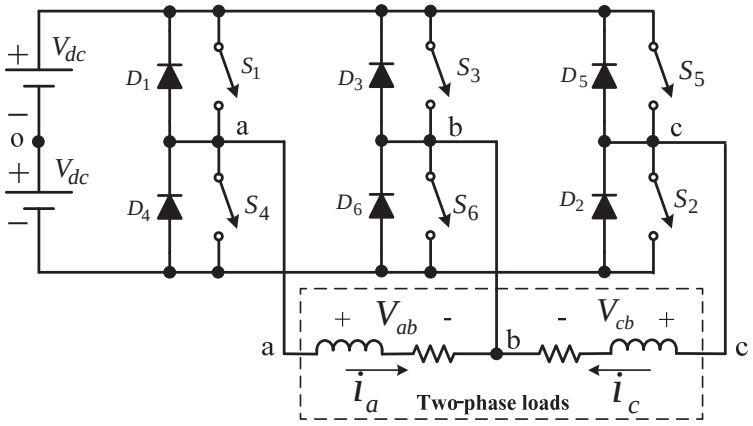


Figure 1. Three-leg VSI supplying two-phase loads.

2. Conventional Space Vector PWM (CSVPWM)

The principle of carrier-based balanced two-phase output voltage SVPWM applied to a three-leg VSI is modified from the conventional three-phase SVPWM[5]. The desired output voltage (V_o^*) and space vector plane can be displayed in Fig.2. The desired balanced output voltage gives a circular trajectory as the dotted line. Mathematical calculation of switching times for the proposed method can be dealt with in the same manner as conventional three-phase SVPWM.

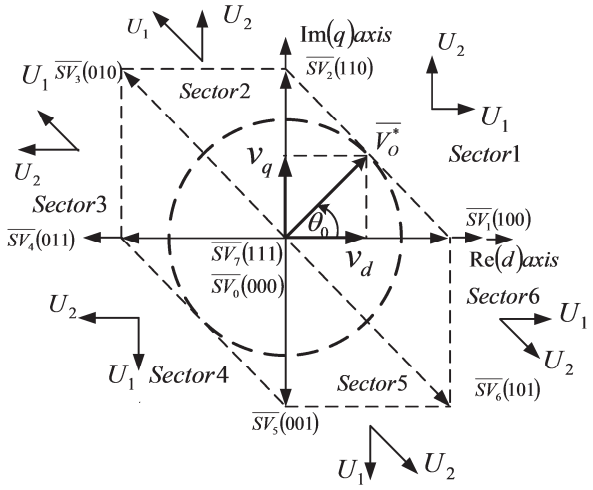


Figure 2. Relationship between active space vectors.

The desired output voltage in vector form which is a rotating vector can be calculated in terms of the average of a number of these space vectors within a switching period in each sector as

$$\overline{V_0^*} = V_0 \angle \theta_0 = \frac{t_1}{\Delta T/2}\overline{U_1} + \frac{t_2}{\Delta T/2}\overline{U_2} \tag{1}$$

when $$\overline{U_1} = V_1 e^{j\alpha_1} \tag{2}$$

$$\overline{U_2} = V_2 e^{j\alpha_2} \tag{3}$$

and $$\frac{\Delta T}{2} = t_1 + t_2 + t_0 + t_7 \tag{4}$$

Note that the sum of active times in each sector is less than the half carrier period (i.e. $t_1 + t_2 \le \Delta T/2$) $\overline{U_1}$ and $\overline{U_2}$ are two basic adjacent vectors; V_1, V_2 are magnitudes of the two basic adjacent space vectors; θ_0 is sampled angular position; α_1, α_2 are angles for the two basic adjacent vectors; t_1, t_2 are active times for the two basic adjacent vectors; t_0, t_7 are times for null vectors; ΔT is a carrier period. Generally, for a symmetrical space vector pattern, space vector time for each zero switching state (t_0, t_7) is set to be equal. For example, Space vector active times (t_1, t_2) for sector 1 are

$$t_1 = \frac{M}{2}\sin\left(\pi/2 - \theta_0\right)\left(\Delta t/2\right) \tag{5}$$

$$t_2 = \frac{M}{2}\sin\left(\theta_0\right)\left(\Delta t/2\right) \tag{6}$$

where $M = \frac{V_o}{V_{dc}}$ is the modulation index, and $0 \le M \le \sqrt{2}$.

The magnitudes of the orthogonal output voltages for the balanced two-phase system can be expressed as

$$V_{ab} = V_{cb} = MV_{dc} \tag{7}$$

3. Proposed Balanced DSVPWM Strategy

DSVPWM for a three-phase system occurs when zero space voltage vectors either $\overline{SV_0}$ (000) or $\overline{SV_7}$ (111) is selected instead of both resulting in removal of zero voltage vector in successive half carrier intervals [1]-[4], [7]. For example, for 120^0 discontinuous modulation, $\overline{SV_0}$ is only selected for all six sectors so-called DPWMMIN (clamp to lower DC rail) for one-third of the fundamental cycle. In the same manner, if $\overline{SV_7}$ is only selected, the zero space vector is continuously locked to the upper DC rail which is called as DPWMMAX. Such both modulation provide clamping and power transfer via switch "ON" to negative and positive bus, respectively. As a result, reduction in one-third fundamental cycle of switching can be achieved. Other modulations such as 60^0 and 30^0 discontinuous modulation places alternate zero space vector voltage for successive 60^0 segments in order to achieve symmetry switching pattern and symmetry of clamping for both dc bus rail. Duration of dc bus clamp is 60^0. The position of zero clamping is at positive and negative peak zone of its fundamental reference voltage which is so-called DPWM 1 which is suitable for resistive load. For 60^0 clamp, the non-switching period occurs at peak zone of the load current with power factor of 0.866 which is RL load resulting in a higher reduction in switching loss than DPWM 1. The types of discontinuous modulation are called DPWM 2 and DPWM 0 for pf of 0.866 lag and pf of 0.866 lead, respectively [3].

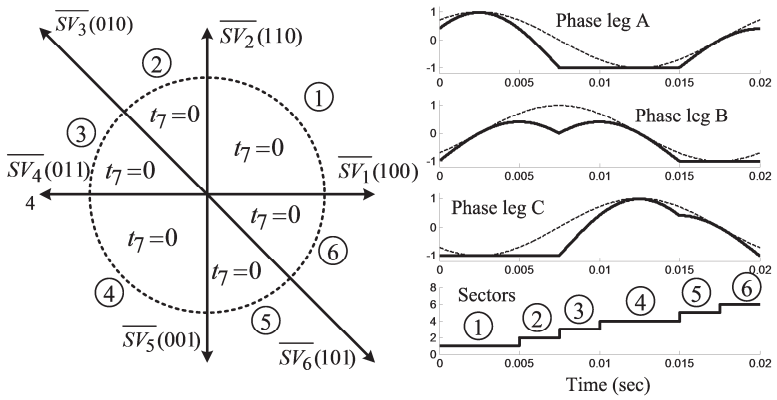
This section describes the proposed DSVPWM. The purposes of this strategy are reductions in switching loss and output current ripple. DSVPWM strategies for balanced two phase output voltages using three-leg VSI are modified from three-phase balanced output voltages using three-leg VSI. The calculation of space vector active times for continuous PWM modulation providing balanced two-phase output voltages has already mentioned in [6]. For analysis of DPWMMIN for balanced output voltages, zero space vector voltage $\overline{SV_0}$ is only selected. The zero space vector time t_0 is

$$t_0 = \frac{\Delta T}{2} - t_1 - t_2 \tag{8}$$

For example, phase-leg reference voltage of phase a in sector 1 is given by

$$v_{ao} = V_{dc}\left[\frac{t_1}{\Delta T/2} + \frac{t_2}{\Delta T/2} - \frac{t_0}{\Delta T/2}\right] \tag{9}$$

Substituting t_1, t_2 and t_0 from Eq. (5), (6) and (8). Locations of active space vector and phase reference waveforms for DPWMMIN are plotted as shown in Figs. 3(a) and (b) respectively.



(a) (b)

Figure 3. Discontinuous PWMMIN (Type 1) (a) Location of active space vectors and placement of zero space vector time and (b) Phase leg reference voltage waveforms in each sector.

Normalized phase-leg reference voltage with the mid-point of phase-leg “a”, “b” and “c” for sector 1 are shown in Eq. (10), (11) and (12)

$$\frac{v_{ao}}{V_{dc}} = M\sin(\frac{\pi}{2} - \theta_o) + M\sin(\theta_o) - 1 \tag{10}$$

$$\frac{v_{bo}}{V_{dc}} = M\sin(\theta_o) - 1 \tag{11}$$

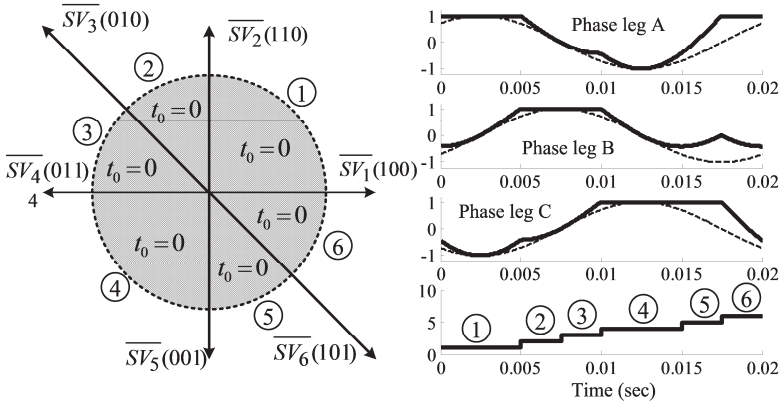
$$\frac{v_{co}}{V_{dc}} = -1 \tag{12}$$

For DPWMMAX, only $\overline{SV_7}$ is chosen. Phase-leg reference voltage functions for sector 1 are shown in Eq. (13)-(14). Phase reference waveforms for DPWMMAX are plotted as shown in Fig. 4.

$$\frac{v_{ao}}{V_{dc}} = +1 \tag{13}$$

$$\frac{v_{bo}}{V_{dc}} = -M\sin(\frac{\pi}{2} - \theta_o) + 1 \tag{14}$$

$$\frac{v_{co}}{V_{dc}} = -M\sin(\frac{\pi}{2} - \theta_o) - M\sin(\theta_o) + 1 \tag{15}$$



(a) (b)

Figure 4. Discontinuous PWMMAX (a) Location of active space vectors and placement of zero space vector time and (b) Phase leg reference voltage waveforms in each sector.

For achieved symmetry switching pulse pattern and symmetry of clamping of both DC bus rail, zero space voltage vector either $\overline{SV_0}$ or $\overline{SV_7}$ is selected in order to reduce the switching loss and current ripple at 30 degrees of load power factor. Voltage and current waveforms at lagging power factor angle of 30 degrees can be plotted in Fig.5. It is found that the clamping zone of peak values for positive and negative cycle of $i_a^{'}$ is at sector 1 and 4, respectively. The clamping zone of peak values for positive and negative cycle of $i_b^{'}$ is at sector 3 and 6, respectively.

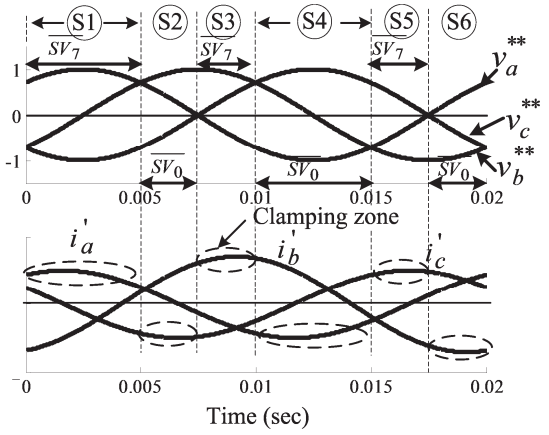
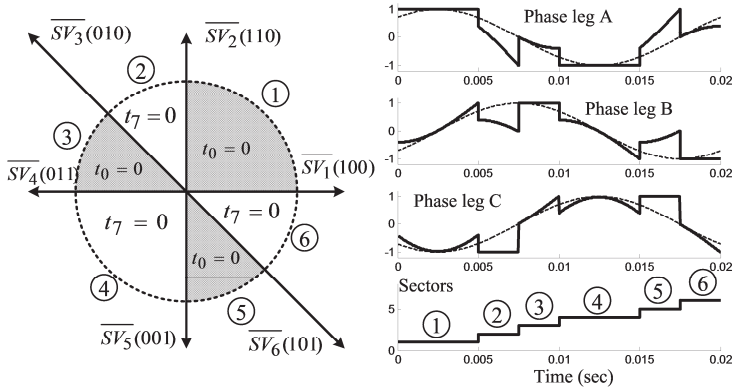


Figure 5. Clamping area at 30^0 lagging power factor for Discontinuous PWM (Type 2).

The area of peak values for positive and negative cycle of $i_c^{'}$ is at sector 5 and 2, respectively. Therefore, 30 degree lagging clamp modulation is defined as Type 2 as shown in Fig.6. $\overline{SV_7}$ is only used in sector 1. $\overline{SV_0}$ is only used for sector 2 as shown in Fig. 6(a). For sector 1, Phase leg reference voltages use equations (13)-(15), and Phase leg reference voltages use equations (10)-(12) for sector 2.



(a) (b)

Figure 6. Discontinuous PWM (Type 2) (a) Location of active space vectors and placement of zero space vector time and (b) Phase leg reference voltage waveforms in each sector.

4. Switching Losses Analysis

For this analysis, conduction loss is not included. Assume that the switching devices have linearity of voltage and current changes during the turn-on and turn-off process. According to the main power circuit in Fig. 1 the resistance of the switch is zero due to conduction loss ignorance. Gate drive signal for turn on and turn off is shown in Fig. 7(a). Waveforms of current flowing pass a switch and voltage across a switch and switching time of each switch are shown in Fig 7(b). Fig. 7(c) shows switching power loss in a switching period [1], [8]. From Fig.7, during turn-on (t_{on}) and turn-off (t_{off}), switch current rises linearly and voltage across switch decreases linearly as a function of times as follows

$$i_{SW}(t) = I_{SW}\frac{t}{t_{on}} \quad ; v_{SW}(t) = 2V_{dc} - 2V_{dc}\frac{t}{t_{on}} \tag{16}$$

When t_{on} is turn-on time. T_{SW} is period of switching. The average switching power loss is

$$P_{on,avg} = \frac{1}{T_{SW}}\int_0^{t_{on}} i_{SW} v_{SW}\, dt = f_{SW} I_{SW} t_{on}\frac{V_{dc}}{3} \tag{17}$$

For turn-off time, instantaneous power loss can be expressed

$$P_{off,avg} = \frac{1}{T_{SW}} \int_0^{t_{off}} P_{off}(t)dt = f_{SW} I_{SW} t_{off} \frac{V_{dc}}{3} \tag{18}$$

Total average switching loss in a switching period is

$$P_{SW,avg} = P_{on,avg} + P_{off,avg} = f_{SW} I_{SW} \left(t_{on} + t_{off}\right) \frac{V_{dc}}{3} \tag{19}$$

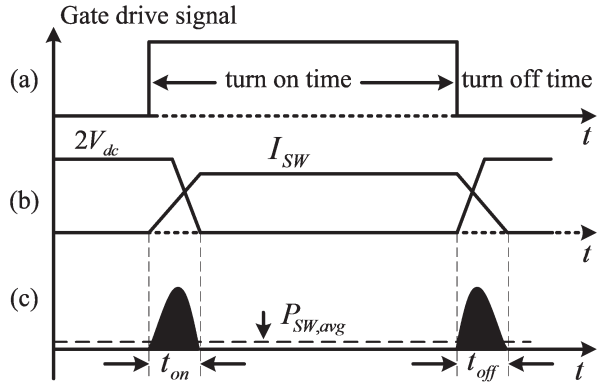


Figure 7. Linearized switching characteristics (a) pulse switching pattern, (b) switching waveforms and (c) instantaneous switching loss.

For the proposed DSVPWM method, switching frequency f_{sw} is 1.5 times switching frequency of continuous SVPWM method [1], [2]. When considering voltage and current of switching devices as shown in Fig.8, Fig. 8(a) illustrates carrier and modulating signals of DSVPWM (Type 1) for upper and lower switching devices in phase-leg a S_1, S_4 of the main power circuit in Fig.1. Waveforms of voltage across S_1, current of S_1 and current of S_4 are shown in Fig.8 (b), (c) and (d), respectively. For time interval between t_4 and t_5, S_4 is on. Therefore, conduction loss occurs in S_4 which is neglected for considering switching loss in phase-leg a devices. Time variant average switching loss waveform over switching period which is dependent of current value I_{SW} and dotted line represents an average of switching loss over a fundamental period are shown in Fig.8 (e). Switching loss during clamp is zero. Therefore, in order to reduce switching loss, clamping can be made at peak zone of the load current.

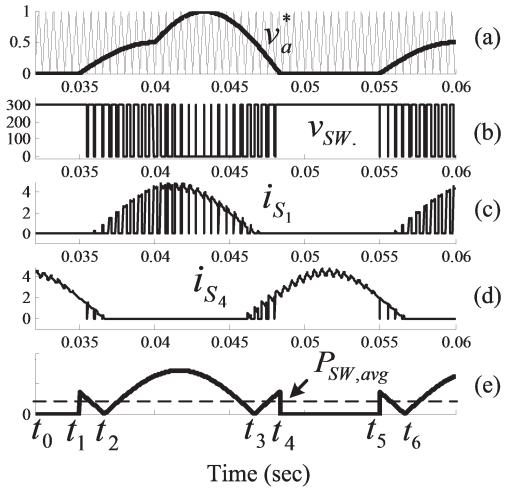


Figure 8. Example of switching waveforms for DPWM (type 1) in phase-leg a (a) modulating signal of phase-leg a, (b) voltage across switching device S_1, (c) current flowing through switching device S_1, (d) current flowing through switching device S_4 and (e) average power switching loss of phase-leg a.

Note that I_{sw} in Fig. 7 for any switching period is assumed constant for determining average switching loss during such interval. For over fundamental period, magnitude of I_{sw} varies with time and relates to the load current. Therefore I_{sw} can be expressed as

$$I_{SW} = \begin{cases} 0 & \text{: unmodulated time} \\ |i_a| & \text{: modulated time} \end{cases} \tag{20}$$

when i_a is the load current of phase-leg a

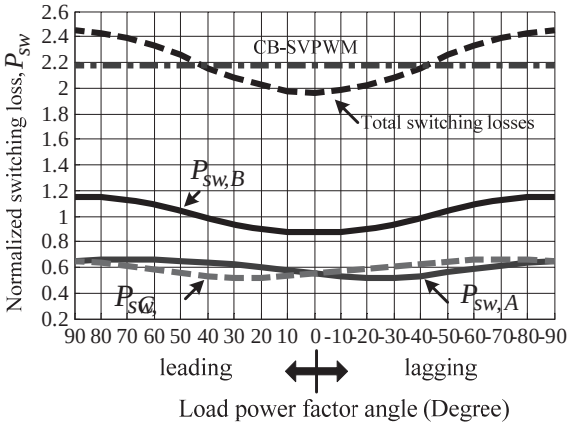


Figure 9. Normalized switching losses of DPWM (type 1).

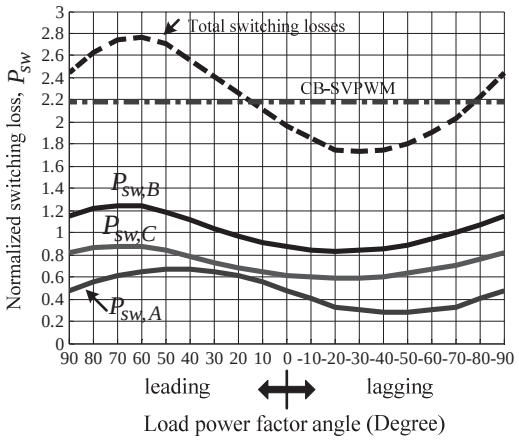


Figure 10. Normalized switching losses of DPWM (type 2).

When considering DSVPWM mentioned earlier, the load power angle varies between 0-90 degrees lagging and 0-90 degrees leading power factor. From Fig. 9, It is found that type 1 gives unequal switching loss for each phase due to unequal angles for each sector. The sum of switching losses of each phase-leg ($P_{sw,A}, P_{sw,B}$ and $P_{sw,C}$) for DPWM (Type 1) is minimum with 1.97 at unity power factor whilst the sum of switching losses of each phase-leg for the conventional balanced phase voltage (CB-SVPWM) is 2.18. The proposed DSVPWM gives 9.6 % reduction of switching loss. DSVPWM type 2 gives minimum switching loss with 1.734 at power angle of 30 degrees. The reduction of switching loss is 20.46 % when compared to CSVPWM.

5. Experimental Results

The overall system for verifying the Discontinuous PWM method is shown in fig. 11. It consists of a 3-phase diode bridge rectifier with filter capacitor providing smooth DC link voltage, a 3-leg voltage source inverter (VSI) converting DC into adjustable voltage and frequency AC, two-phase R-L series circuit acting as a load. The VSI employs IGBTs as semiconductor switches. Modulated signals for driving all IGBTs are generated by Digital signal processor TMS320F28335 eZdsp board together with MATLAB/SIMULINK. DC bus voltage is 300V resulting in voltage across each capacitor of 150 V. A R-L Load has resistance of $35\,\Omega$ and inductance of 50mH to obtain 0.866 lagging load power factor (i.e. 30 degrees power factor angle). The load current lags 30 degrees with respect to fundamental voltage. This condition is required for testing of minimum switching loss. Testing condition has two parts: 1) comparison of switching loss for each condition of CB-SVPWM, Type 1, Type 2 ;2) comparison of output current ripple load current i_a for each condition of CB-SVPWM, type 1 and type 2. Figs. 12-13 show waveforms of reference voltage, phase leg voltage with respect to the midpoint of DC bus, output phase current for each phase having 0.866 load power factor as mentioned earlier. Figs.14-15 are analysis of normalized

power switching loss for each phase of Type 1 and Type 2. Related to voltages and currents for each phase, measured data of voltages and currents for each phase is used for mathematically calculating by using MATLAB/SIMULINK.

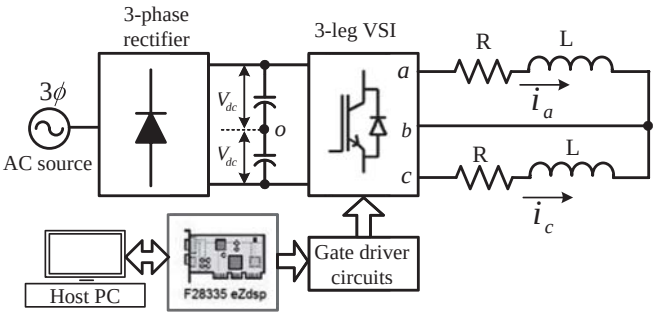


Figure 11. Overall proposed system.

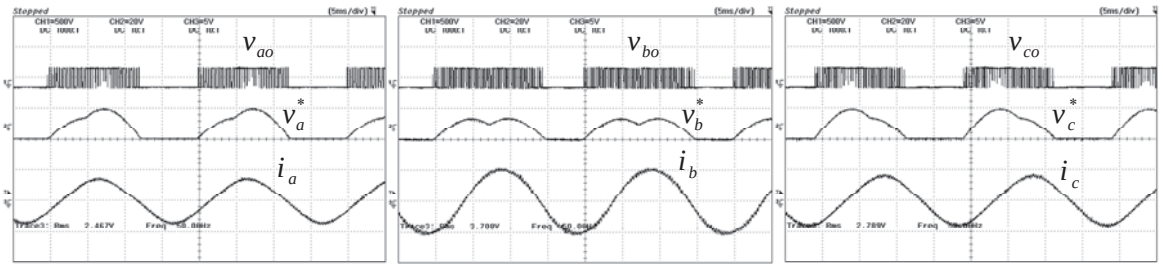


Figure 12. Balanced DSVPWM (Type 1).

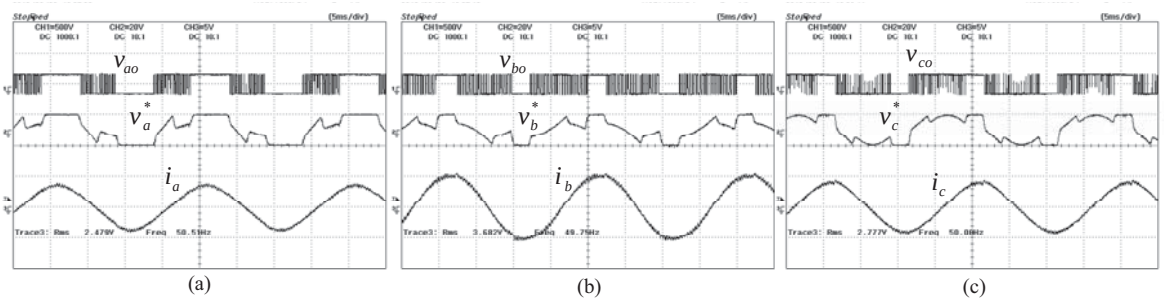


Figure 13. Balanced DSVPWM (Type 2).

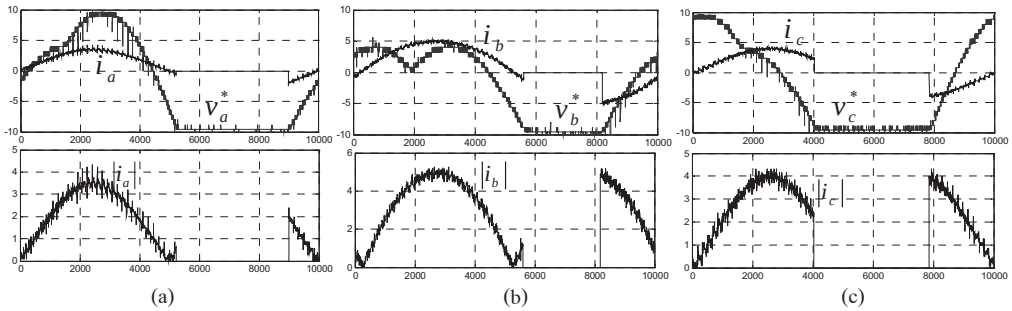


Figure 14. Switching losses of balanced output voltage (Type 1).

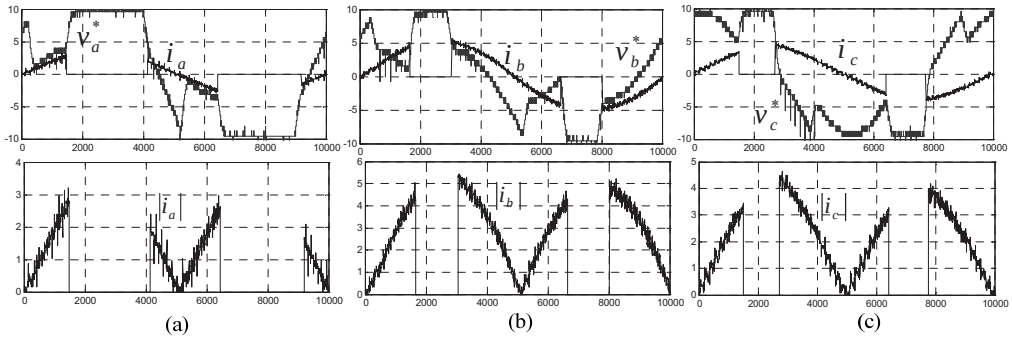


Figure 15. Switching losses of balanced output voltage (Ttpe 2).

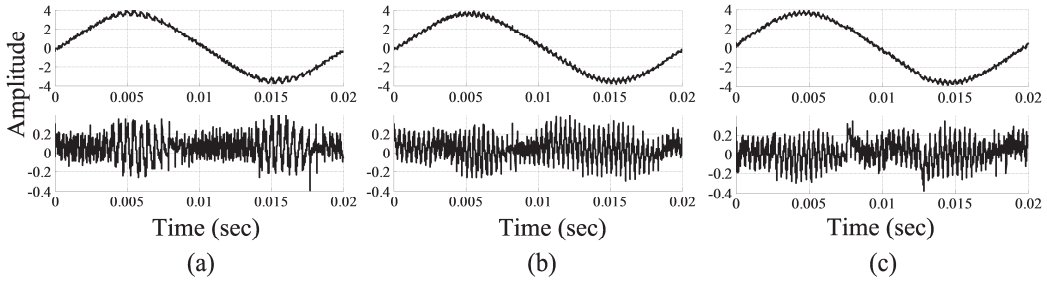


Figure 16. Measured load current ripple of phase leg a (ia) in each type at modulation index = 1.414, F_1 = 50Hz, f_{SW}= 2kHz for CSVPWM and f_{SW}= 3kHz for DSVPWM (a) CSVPWM, (b) type 1 and (c) type2. The measured mean square of load current (ia) are (a) 0.01425, (b) 0.01184 and (c) 0.01198.

The data was collected at fundamental frequency of 50Hz or 2ms/div and sampling rate of 500 kHz. 10,000 sampled data was used. After that phase leg currents were performed to be absolute: $|i_a|$, $|i_b|$ and $|i_c|$. Absolute current value is zero when clamping occurs at positive and negative reference voltage. Average absolute current was used as normalized power switching loss for the analysis of switching loss for each type. Table 1 illustrates normalized power switching losses derived from the average of $|i_a|$, $|i_b|$ and $|i_c|$. The total of average switching losses in type 2 is minimum.

Table 1. Normalized power switching losses.

Method	*Ph.-leg a*	*Ph.-leg b*	*Ph.-leg c*	*Total*
CSVPWM	2.20	3.31	2.50	8.01
TYPE 1	1.76	3.42	2.42	7.6
TYPE 2	0.81	2.97	2.31	6.09

Testing of current ripple considers comparison between continuous SVPWM and discontinuous SVPWM. Current waveforms of i_a and ripple is shown in Fig.16. The ripple currents are extracted from currents excluding fundamental components using MATLAB/SIMULINK.

6. Conclusion

A DSVPWM technique for a two-phase voltage source inverter supplying balanced two-phase loads has been proposed. The proposed type 1 DSVPWM suits a pure restive load. Proposed type 2 is suitable for R-L Load with 30 degree lagging power factor angle. These DSPWM techniques offer a reduction of switching loss and load current ripple at high modulation indices when compared with continuous SVPWM techniques. The validity of the proposed technique are verified by simulation and experimental results in terms of current waveforms, a reduction in switching losses and output current ripple.

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